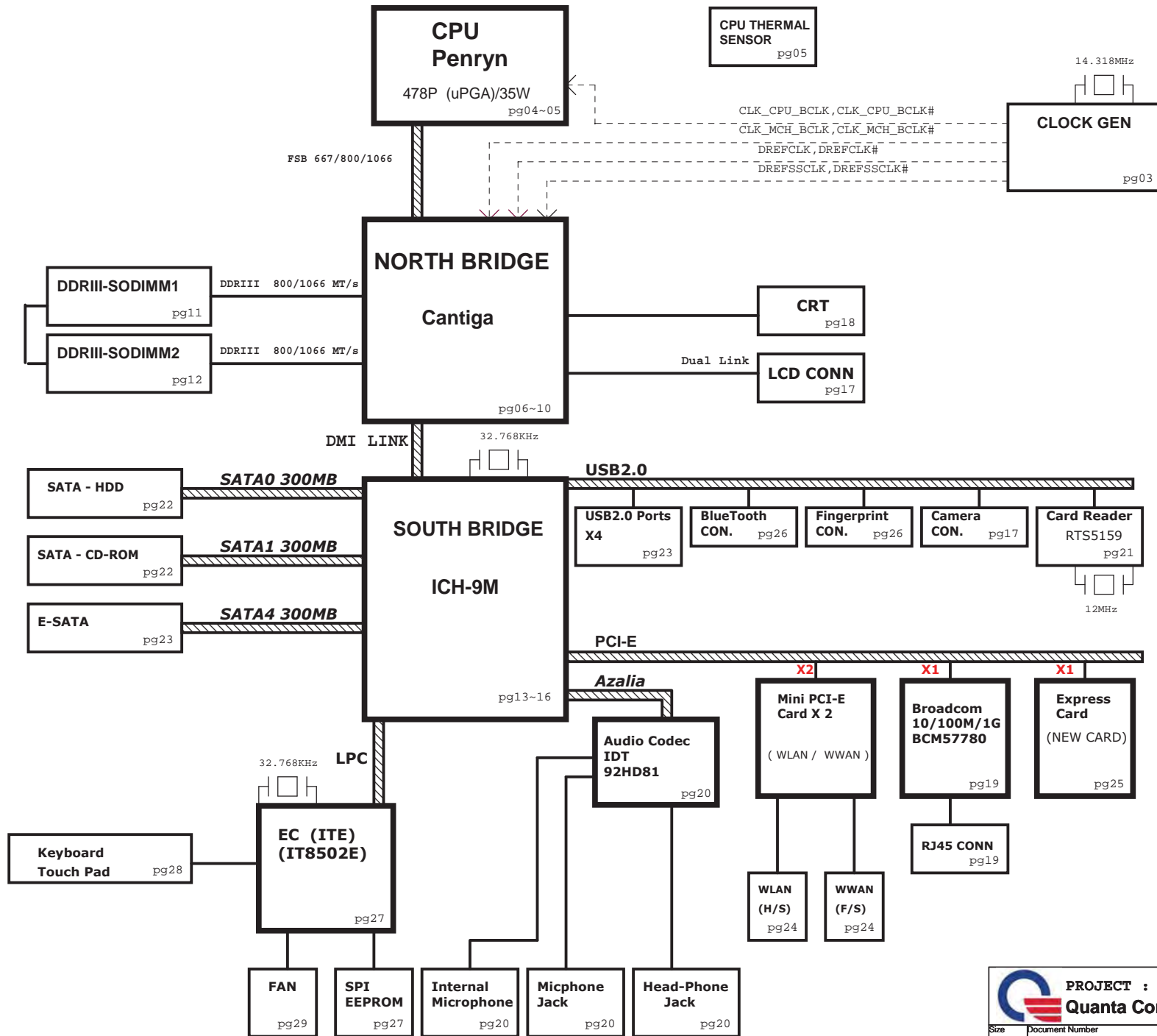



LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



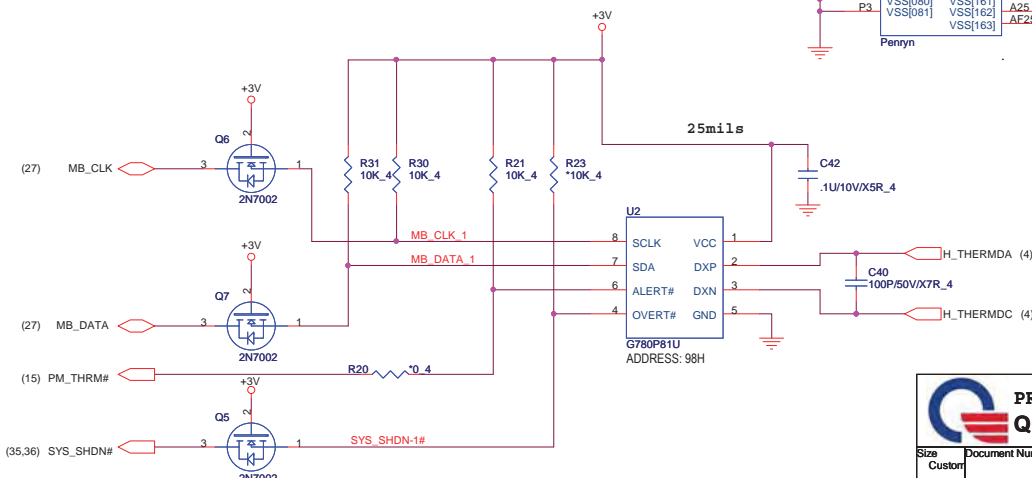
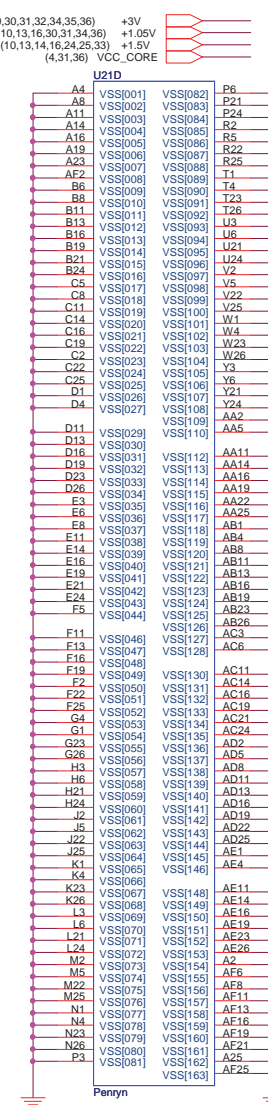
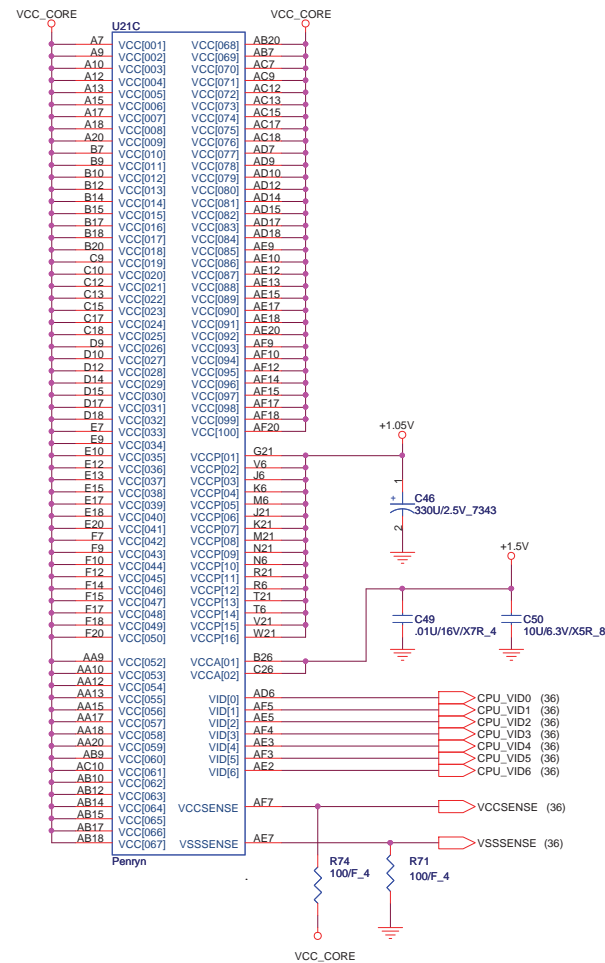
Power States

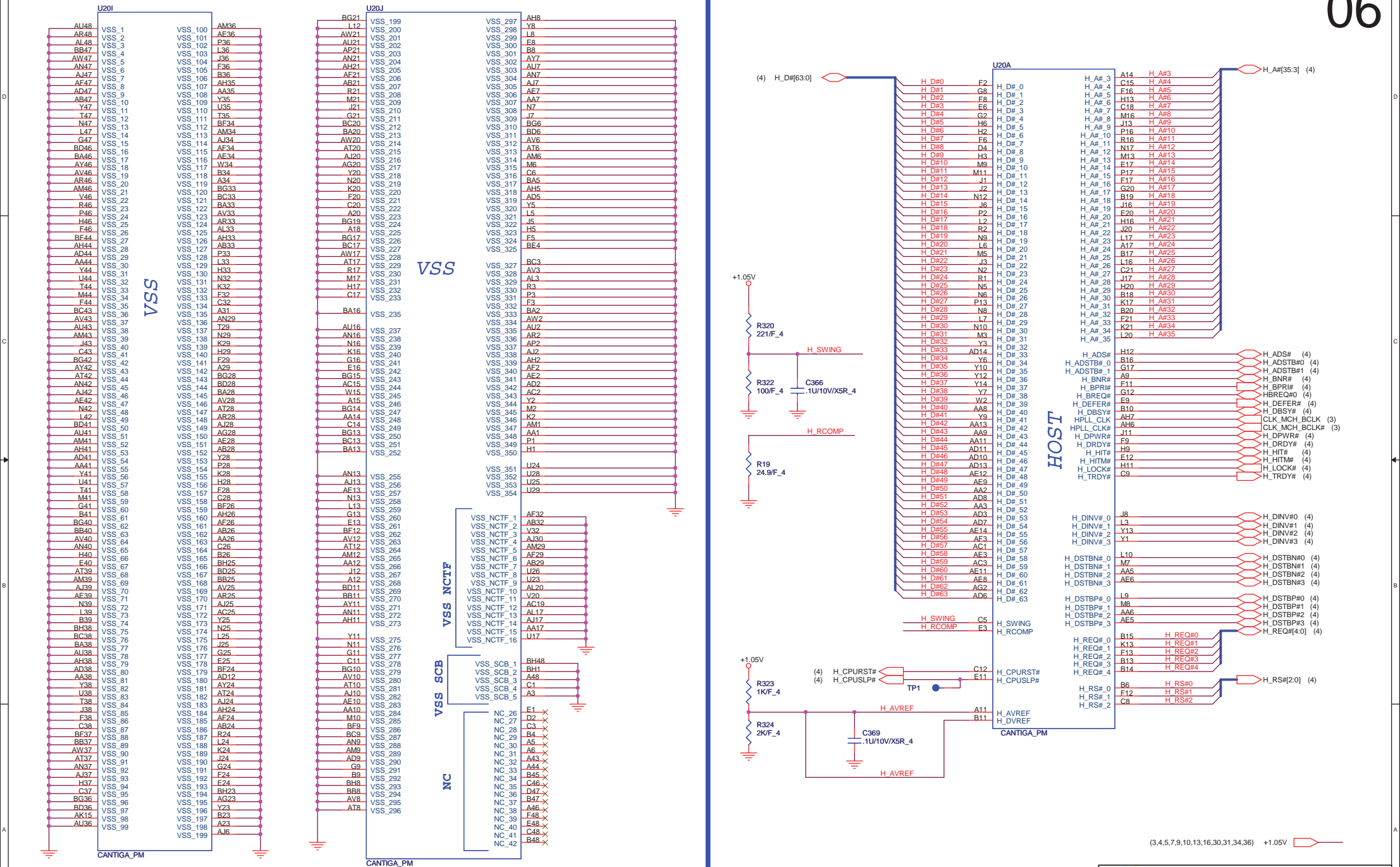
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	18,33,34,35,36,37,38,39	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	13,16,32	RTC		S0~S5
3VPCU	+3.3V	13,18,22,24,30,32,33,34,36,37	8051 POWER		S0~S5
5VPCU	+5V	30,33,34,35,36,37,38	LCD/CHARGE POWER		S0~S5
+15V	+15V	18,26,33,37	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	22,33	LAN POWER	LAN_ON	
5VSUS	+5V	18,30,33,38	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	14,15,27,28,29,32,33,38	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	10,33,36		SUSON	
1.5VSUS	+1.5V	07,09,10,11,12,33,35	SODIMM POWER CALISTOGA/ICH8 POWER	SUSON	
SMDDR_VREF_DIMM	+0.75V	11,12	SODIMM POWER		
+5V	+5V	16,17,18,19,21,23,24,25,32,33,34	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	03,05,07,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38	SLP_S3# CTRLD POWER	MAINON	
+1.5V	+1.5V	05,10,13,14,15,16,21,27,28,29,35	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	03,04,05,06,07,09,10,13,16,33,36,38	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	04,05,33,38	CPU CORE POWER	VRON	
LCDVCC	+3.3V	18	LCD Power	INT_DISP_ON	
+5VHDD	+5V	23	HDD Power	MAINON	
MBATV	+10V~+17V	32,34	MAIN BATTERY	D/C#	

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		Quanta Computer Inc.	
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		FRON TPAGE	
Date: Wednesday, July 15, 2009		Sheet 2 of 36	









MCH_CFG_5 DMIX2 selection

Low: DMIX2

High: DMIX4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled

High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane

High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)

High: Lane Reversed

MCH_CFG_6 TPM Host Interface

Low: TPM Host Interface enabled

High: TPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low = Intel Management Engine Crypto Transport

Layer Security (TLS) cipher suite with no

confidentiality

High = Intel Management Engine Crypto TLS cipher

suite with confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled

High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_12 MCH_CFG_13 Configuration

0 0 Reserved

1 0 XOR Mode enabled

0 1 All-Z Mode enabled

1 1 Normal operation (Default)

TP16 AL34

TP17 AK34

TP18 AN35

TP20 AM35

(3) MCH_BSEL0

(3) MCH_BSEL1

(3) MCH_BSEL2

TP5 MCH_CFG_3

TP6 MCH_CFG_4

R43 MCH_CFG_5

R42 MCH_CFG_6

R41 MCH_CFG_7

R38 MCH_CFG_8

R40 MCH_CFG_9

R37 MCH_CFG_10

R36 MCH_CFG_11

R39 MCH_CFG_12

TP7 MCH_CFG_13

TP9 MCH_CFG_14

TP11 MCH_CFG_15

TP12 MCH_CFG_16

TP13 MCH_CFG_17

TP14 MCH_CFG_18

TP15 MCH_CFG_19

TP16 MCH_CFG_20

R52 MCH_CFG_21

R53 MCH_CFG_22

R54 MCH_CFG_23

R55 MCH_CFG_24

R56 MCH_CFG_25

R57 MCH_CFG_26

R58 MCH_CFG_27

R59 MCH_CFG_28

R60 MCH_CFG_29

R61 MCH_CFG_30

R62 MCH_CFG_31

R63 MCH_CFG_32

R64 MCH_CFG_33

R65 MCH_CFG_34

R66 MCH_CFG_35

R67 MCH_CFG_36

R68 MCH_CFG_37

R69 MCH_CFG_38

R70 MCH_CFG_39

R71 MCH_CFG_40

R72 MCH_CFG_41

R73 MCH_CFG_42

R74 MCH_CFG_43

R75 MCH_CFG_44

R76 MCH_CFG_45

R77 MCH_CFG_46

R78 MCH_CFG_47

R79 MCH_CFG_48

R80 MCH_CFG_49

R81 MCH_CFG_50

R82 MCH_CFG_51

R83 MCH_CFG_52

R84 MCH_CFG_53

R85 MCH_CFG_54

R86 MCH_CFG_55

R87 MCH_CFG_56

R88 MCH_CFG_57

R89 MCH_CFG_58

R90 MCH_CFG_59

R91 MCH_CFG_60

R92 MCH_CFG_61

R93 MCH_CFG_62

R94 MCH_CFG_63

R95 MCH_CFG_64

R96 MCH_CFG_65

R97 MCH_CFG_66

R98 MCH_CFG_67

R99 MCH_CFG_68

R100 MCH_CFG_69

R101 MCH_CFG_70

R102 MCH_CFG_71

R103 MCH_CFG_72

R104 MCH_CFG_73

R105 MCH_CFG_74

R106 MCH_CFG_75

R107 MCH_CFG_76

R108 MCH_CFG_77

R109 MCH_CFG_78

R110 MCH_CFG_79

R111 MCH_CFG_80

R112 MCH_CFG_81

R113 MCH_CFG_82

R114 MCH_CFG_83

R115 MCH_CFG_84

R116 MCH_CFG_85

R117 MCH_CFG_86

R118 MCH_CFG_87

R119 MCH_CFG_88

R120 MCH_CFG_89

R121 MCH_CFG_90

R122 MCH_CFG_91

R123 MCH_CFG_92

R124 MCH_CFG_93

R125 MCH_CFG_94

R126 MCH_CFG_95

R127 MCH_CFG_96

R128 MCH_CFG_97

R129 MCH_CFG_98

R130 MCH_CFG_99

R131 MCH_CFG_100

R132 MCH_CFG_101

R133 MCH_CFG_102

R134 MCH_CFG_103

R135 MCH_CFG_104

R136 MCH_CFG_105

R137 MCH_CFG_106

R138 MCH_CFG_107

R139 MCH_CFG_108

R140 MCH_CFG_109

R141 MCH_CFG_110

R142 MCH_CFG_111

R143 MCH_CFG_112

R144 MCH_CFG_113

R145 MCH_CFG_114

R146 MCH_CFG_115

R147 MCH_CFG_116

R148 MCH_CFG_117

R149 MCH_CFG_118

R150 MCH_CFG_119

R151 MCH_CFG_120

R152 MCH_CFG_121

R153 MCH_CFG_122

R154 MCH_CFG_123

R155 MCH_CFG_124

R156 MCH_CFG_125

R157 MCH_CFG_126

R158 MCH_CFG_127

R159 MCH_CFG_128

R160 MCH_CFG_129

R161 MCH_CFG_130

R162 MCH_CFG_131

R163 MCH_CFG_132

R164 MCH_CFG_133

R165 MCH_CFG_134

R166 MCH_CFG_135

R167 MCH_CFG_136

R168 MCH_CFG_137

R169 MCH_CFG_138

R170 MCH_CFG_139

R171 MCH_CFG_140

R172 MCH_CFG_141

R173 MCH_CFG_142

R174 MCH_CFG_143

R175 MCH_CFG_144

R176 MCH_CFG_145

R177 MCH_CFG_146

R178 MCH_CFG_147

R179 MCH_CFG_148

R180 MCH_CFG_149

R181 MCH_CFG_150

R182 MCH_CFG_151

R183 MCH_CFG_152

R184 MCH_CFG_153

R185 MCH_CFG_154

R186 MCH_CFG_155

R187 MCH_CFG_156

R188 MCH_CFG_157

R189 MCH_CFG_158

R190 MCH_CFG_159

R191 MCH_CFG_160

R192 MCH_CFG_161

R193 MCH_CFG_162

R194 MCH_CFG_163

R195 MCH_CFG_164

R196 MCH_CFG_165

R197 MCH_CFG_166

R198 MCH_CFG_167

R199 MCH_CFG_168

R200 MCH_CFG_169

R201 MCH_CFG_170

R202 MCH_CFG_171

R203 MCH_CFG_172

R204 MCH_CFG_173

R205 MCH_CFG_174

R206 MCH_CFG_175

R207 MCH_CFG_176

R208 MCH_CFG_177

R209 MCH_CFG_178

R210 MCH_CFG_179

R211 MCH_CFG_180

R212 MCH_CFG_181

R213 MCH_CFG_182

R214 MCH_CFG_183

R215 MCH_CFG_184

R216 MCH_CFG_185

R217 MCH_CFG_186

R218 MCH_CFG_187

R219 MCH_CFG_188

R220 MCH_CFG_189

R221 MCH_CFG_190

R222 MCH_CFG_191

R223 MCH_CFG_192

R224 MCH_CFG_193

R225 MCH_CFG_194

R226 MCH_CFG_195

R227 MCH_CFG_196

R228 MCH_CFG_197

R229 MCH_CFG_198

R230 MCH_CFG_199

R231 MCH_CFG_200

R232 MCH_CFG_201

R233 MCH_CFG_202

R234 MCH_CFG_203

R235 MCH_CFG_204

R236 MCH_CFG_205

R237 MCH_CFG_206

R238 MCH_CFG_207

R239 MCH_CFG_208

R240 MCH_CFG_209

R241 MCH_CFG_210

R242 MCH_CFG_211

R243 MCH_CFG_212

R244 MCH_CFG_213

R245 MCH_CFG_214

R246 MCH_CFG_215

R247 MCH_CFG_216

R248 MCH_CFG_217

R249 MCH_CFG_218

R250 MCH_CFG_219

R251 MCH_CFG_220

R252 MCH_CFG_221

R253 MCH_CFG_222

R254 MCH_CFG_223

R255 MCH_CFG_224

R256 MCH_CFG_225

R257 MCH_CFG_226

R258 MCH_CFG_227

R259 MCH_CFG_228

R260 MCH_CFG_229

R261 MCH_CFG_230

R262 MCH_CFG_231

R263 MCH_CFG_232

R264 MCH_CFG_233

R265 MCH_CFG_234

R266 MCH_CFG_235

R267 MCH_CFG_236

R268 MCH_CFG_237

R269 MCH_CFG_238

R270 MCH_CFG_239

R271 MCH_CFG_240

R272 MCH_CFG_241

R273 MCH_CFG_242

R274 MCH_CFG_243

R275 MCH_CFG_244

R276 MCH_CFG_245

R277 MCH_CFG_246

R278 MCH_CFG_247

R279 MCH_CFG_248

R280 MCH_CFG_249

R281 MCH_CFG_250

R282 MCH_CFG_251

R283 MCH_CFG_252

R284 MCH_CFG_253

R285 MCH_CFG_254

R286 MCH_CFG_255

R287 MCH_CFG_256

R288 MCH_CFG_257

R289 MCH_CFG_258

R290 MCH_CFG_259

R291 MCH_CFG_260

R292 MCH_CFG_261

R293 MCH_CFG_262

R294 MCH_CFG_263

R295 MCH_CFG_264

R296 MCH_CFG_265

R297 MCH_CFG_266

R298 MCH_CFG_267

R299 MCH_CFG_268

R300 MCH_CFG_269

R301 MCH_CFG_270

R302 MCH_CFG_271

R303 MCH_CFG_272

R304 MCH_CFG_273

R305 MCH_CFG_274

R306 MCH_CFG_275

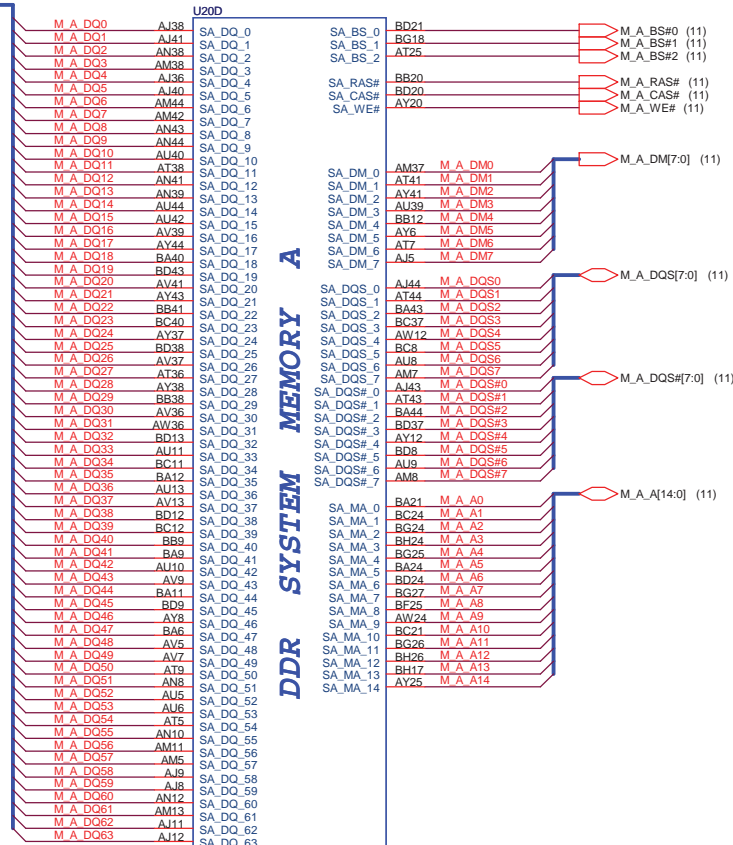
R307 MCH_CFG_276

R308 MCH_CFG_277

R309 MCH_CFG_278

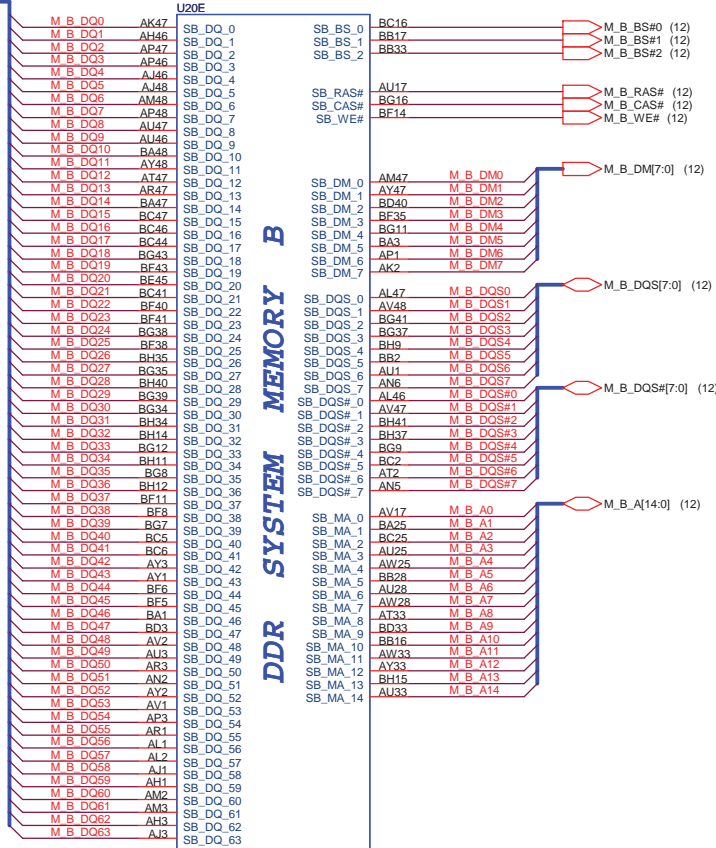
R310 MCH

(11) M_A_DQ[63:0]



CANTIGA_PM

(12) M_B_DQ[63:0]

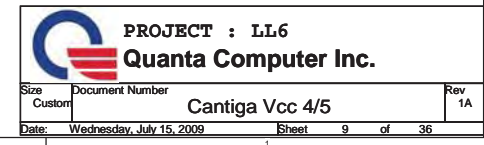


CANTIGA_PM

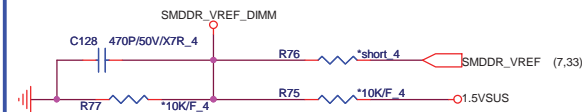
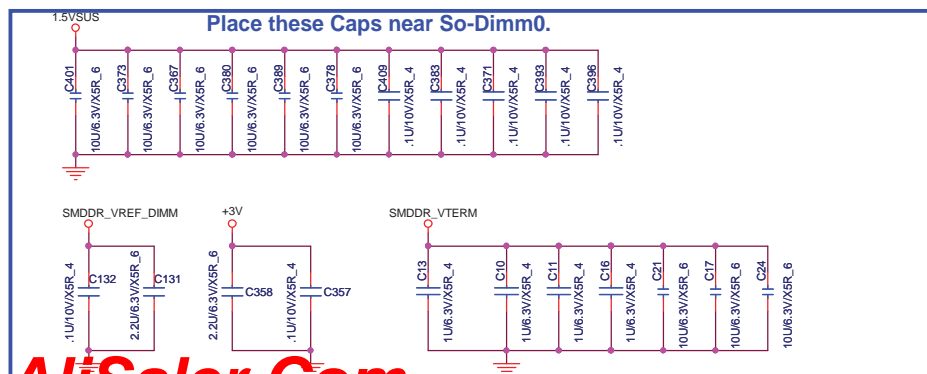
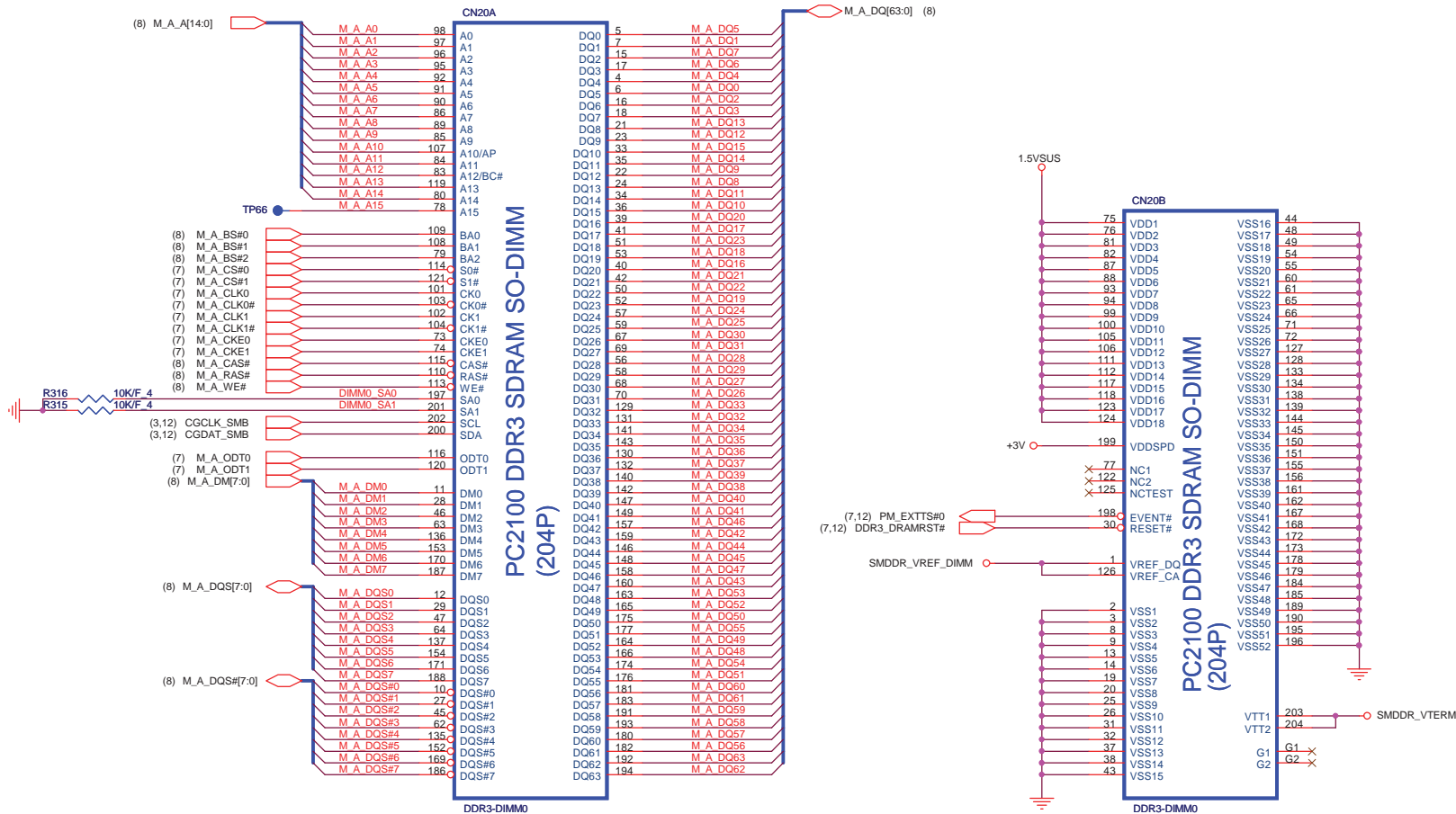


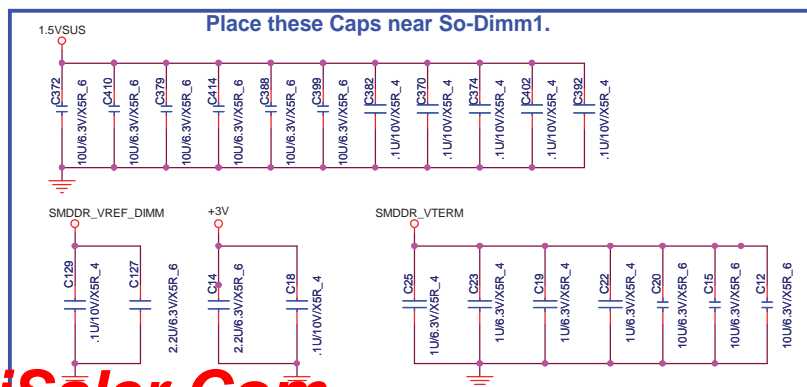
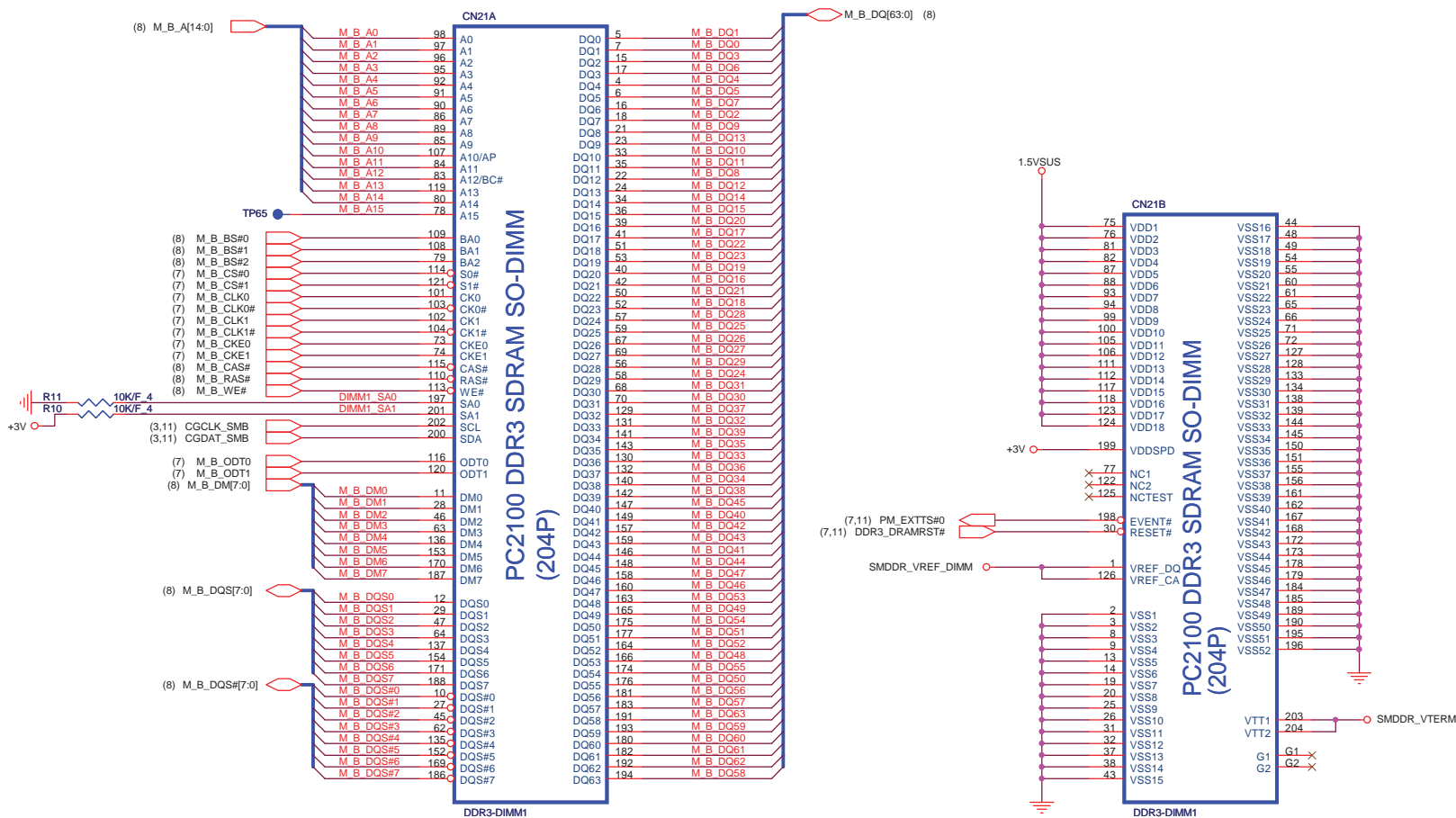
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Quanta Computer Inc.

Size: Custom Document Number: Cantiga DDR3 3/5 Rev 1A
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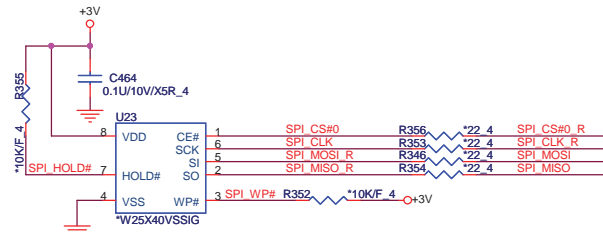
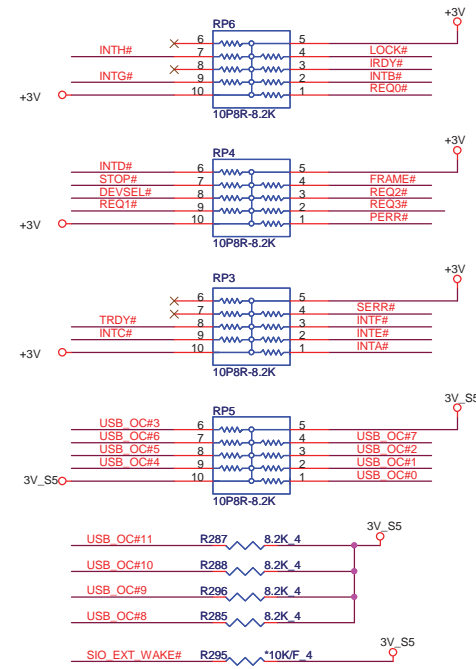
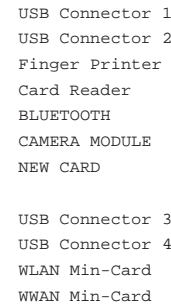




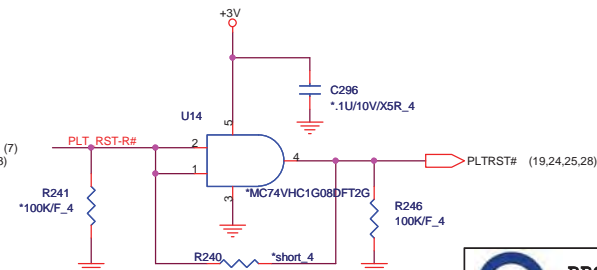
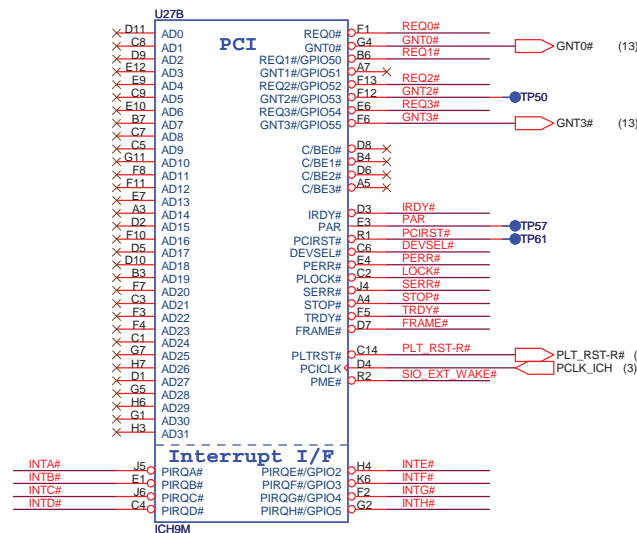




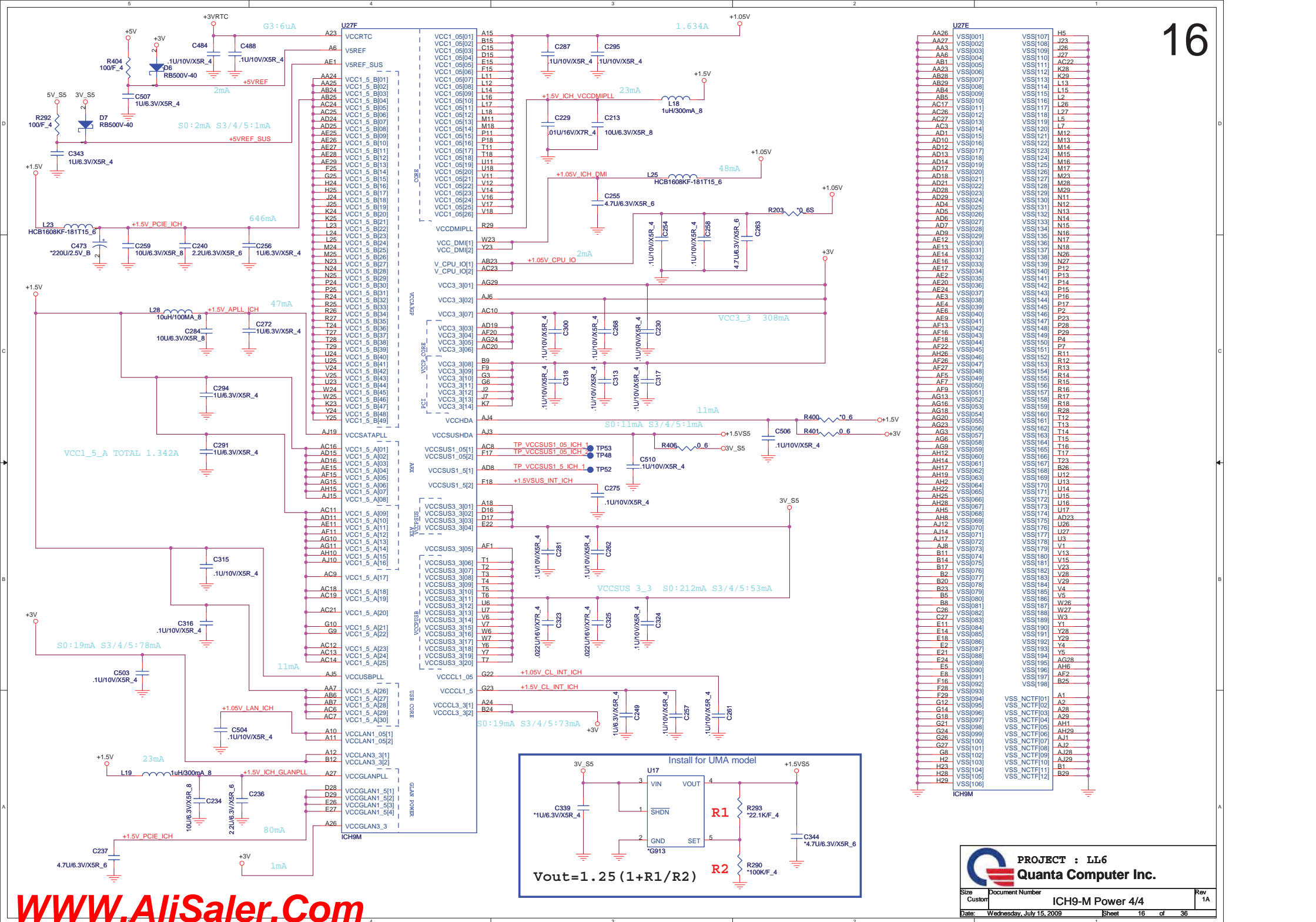
PCIE-LAN



512K byte SPI ROM
For HDCP only

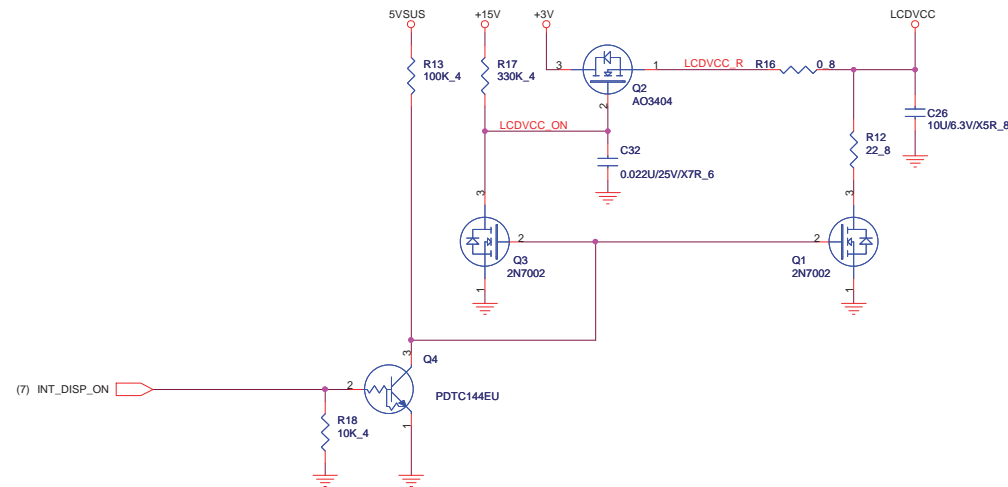




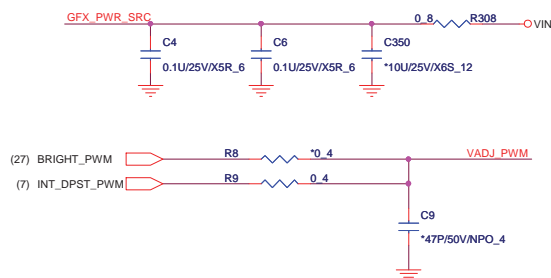
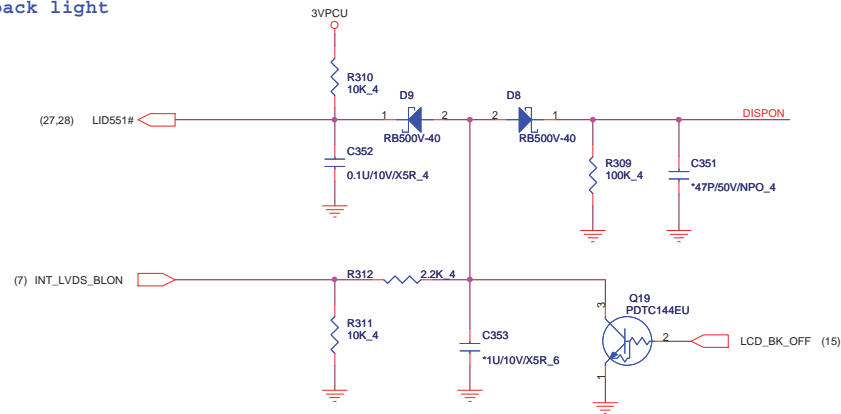


LCD panel control & connector

LCDVCC

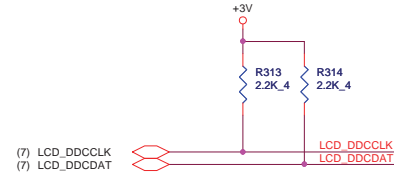


back light

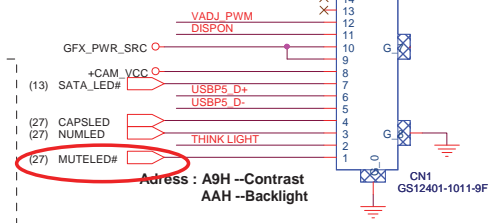
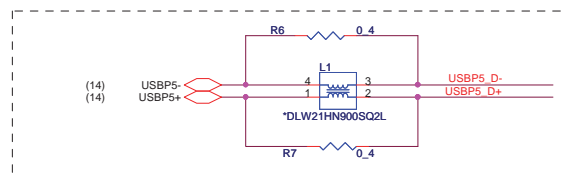


(3,5,7,10,11,12,13,14,15,16,18,19,20,21,22,23,24,25,26,27,28,29,30,31,32,34,35,36)
 (22,31,33,35) +3V
 (31,36) +15V
 (13,19,22,27,28,29,31,32,34,35) 5VSUS
 (30,32,33,34,35,36) 3VPCU
 VIN
 (16,18,20,22,26,27,28,29,30,31,32) +5V

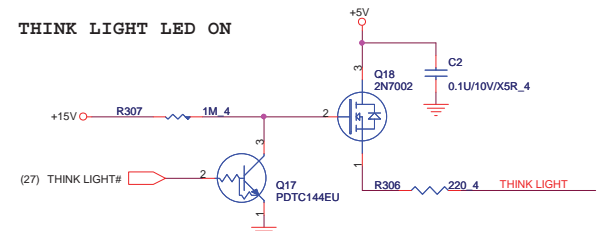
17



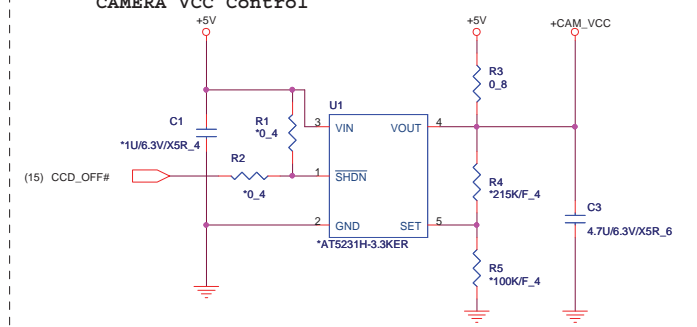
(7) LA_DATAN0 LA_DATAN0
 (7) LA_DATAP0 LA_DATAP0
 (7) LA_DATAN1 LA_DATAN1
 (7) LA_DATAP1 LA_DATAP1
 (7) LA_DATAN2 LA_DATAN2
 (7) LA_DATAP2 LA_DATAP2
 (7) LA_CLK# LA_CLK#
 (7) LA_CLK LA_CLK



THINK LIGHT LED ON



CAMERA VCC Control



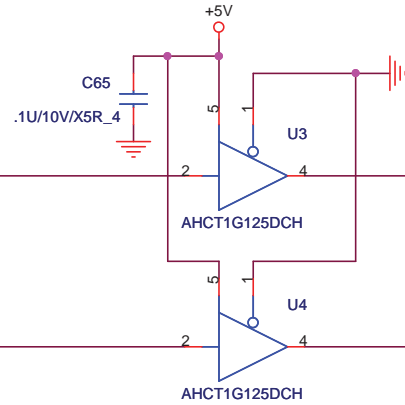
CRT PORT

(7) INT_CRT_RED
(7) INT_CRT_GRN
(7) INT_CRT_BLU

R68
150/F_4
R62
150/F_4
R57
150/F_4
5.6P/50V/COG_4
C102
5.6P/50V/COG_4
C90
5.6P/50V/COG_4
C83
5.6P/50V/COG_4
C82
5.6P/50V/COG_4
C89
5.6P/50V/COG_4
C101
5.6P/50V/COG_4

(7) INT_VSYNC

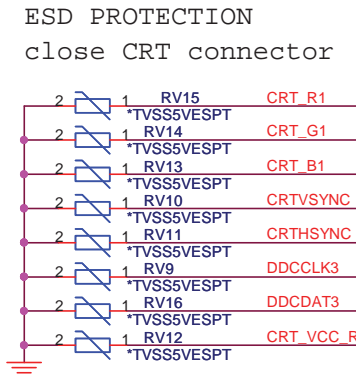
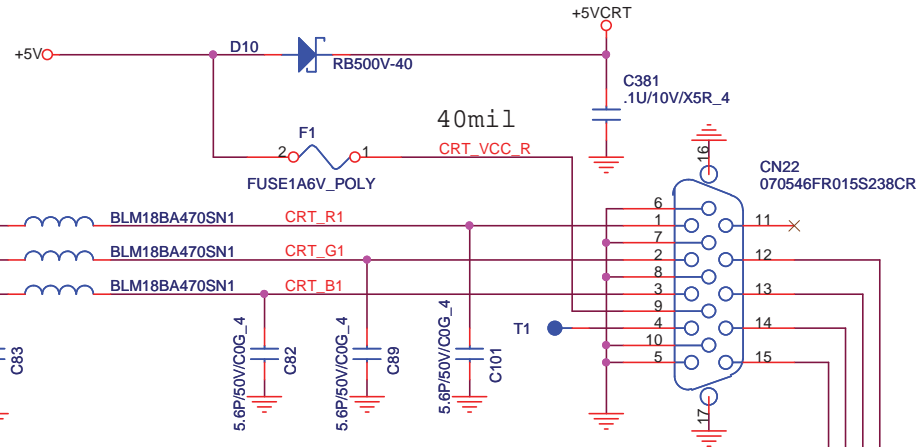
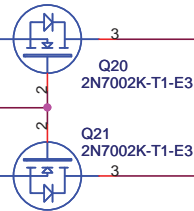
(7) INT_HSYNC




(7) INT_CRT_DDCCLK

(7) INT_CRT_DDCDAT

R337
2.2K_4
R326
2.2K_4
+3V
Q20
2N7002K-T1-E3
+3V
Q21
2N7002K-T1-E3

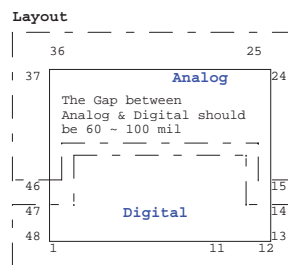
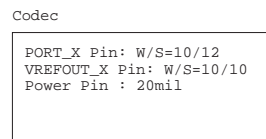
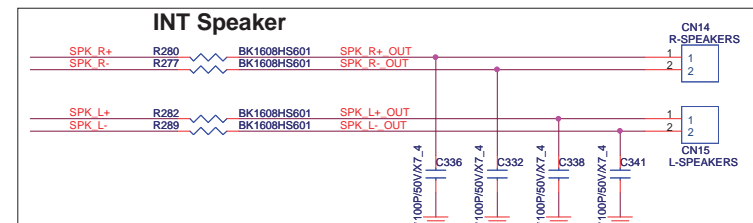




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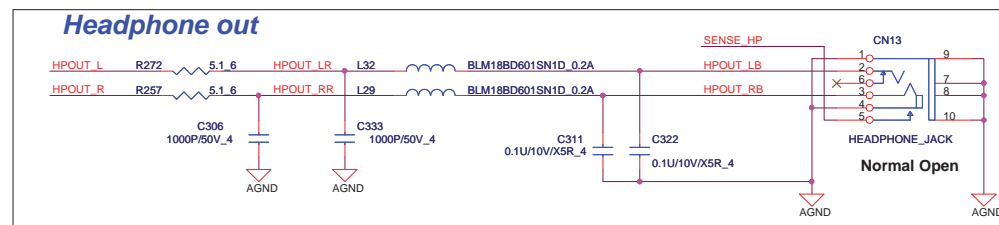
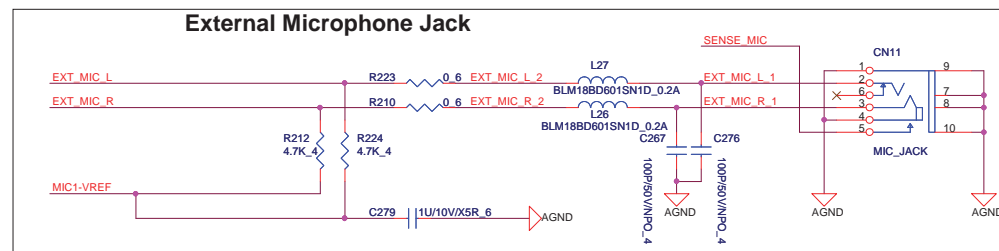
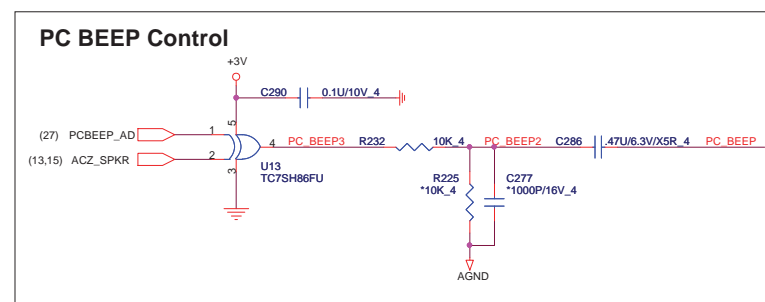
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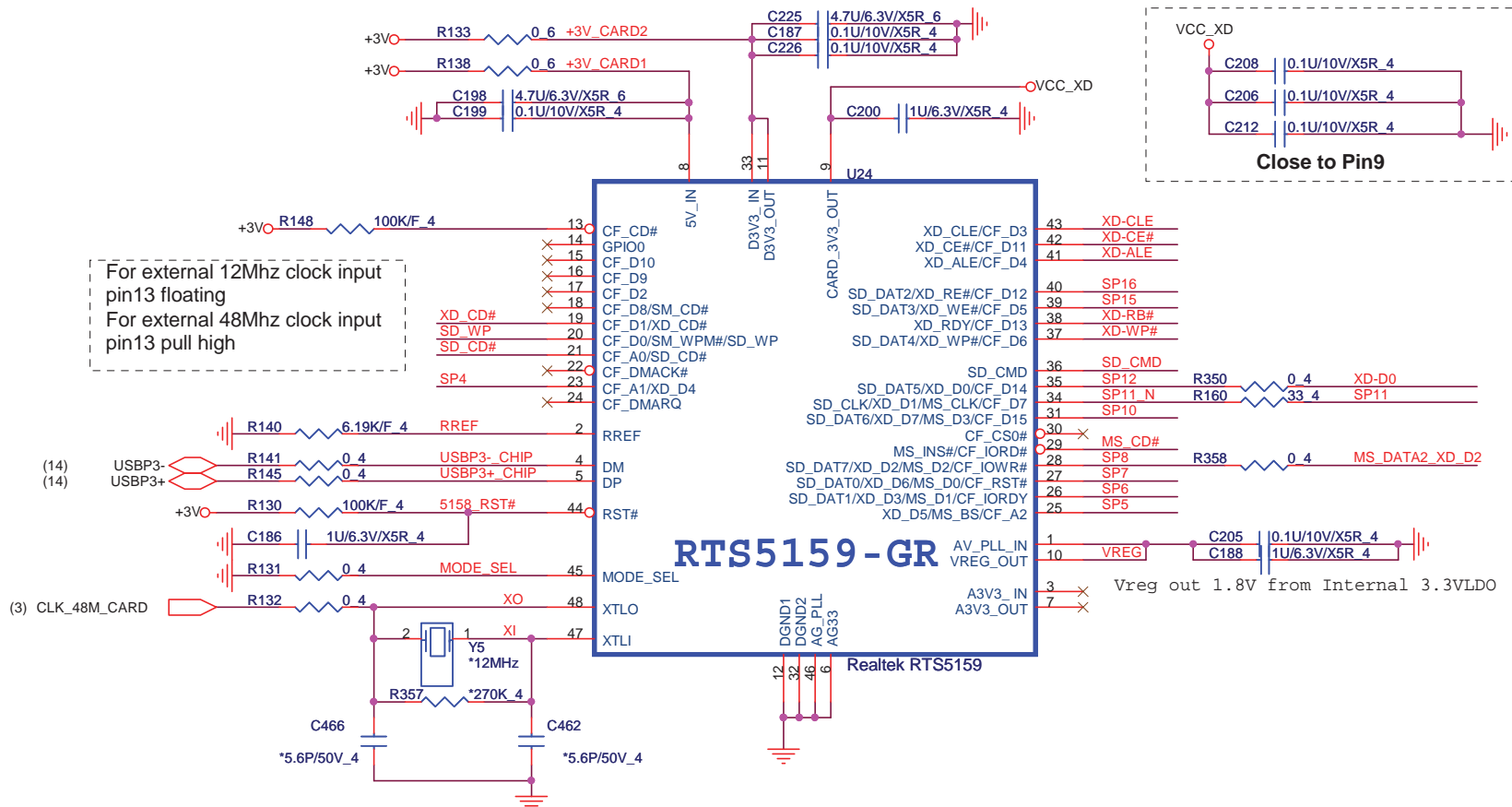




EMI Reserved

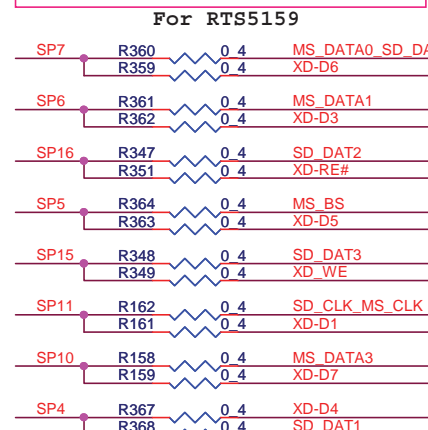
The image displays four identical circuit diagrams, each representing an EMI reserved component. Each diagram consists of a red triangle symbol labeled 'AGND' on the left, connected by a red line to a blue zigzag resistor symbol. The resistor is labeled with its part number (R207, R276, R206, or R291) in red. To the right of the resistor is a red line leading to a label '*SHORT' in red. Below the '*SHORT' label is a ground symbol, which is a horizontal line with three downward-pointing lines of decreasing width.



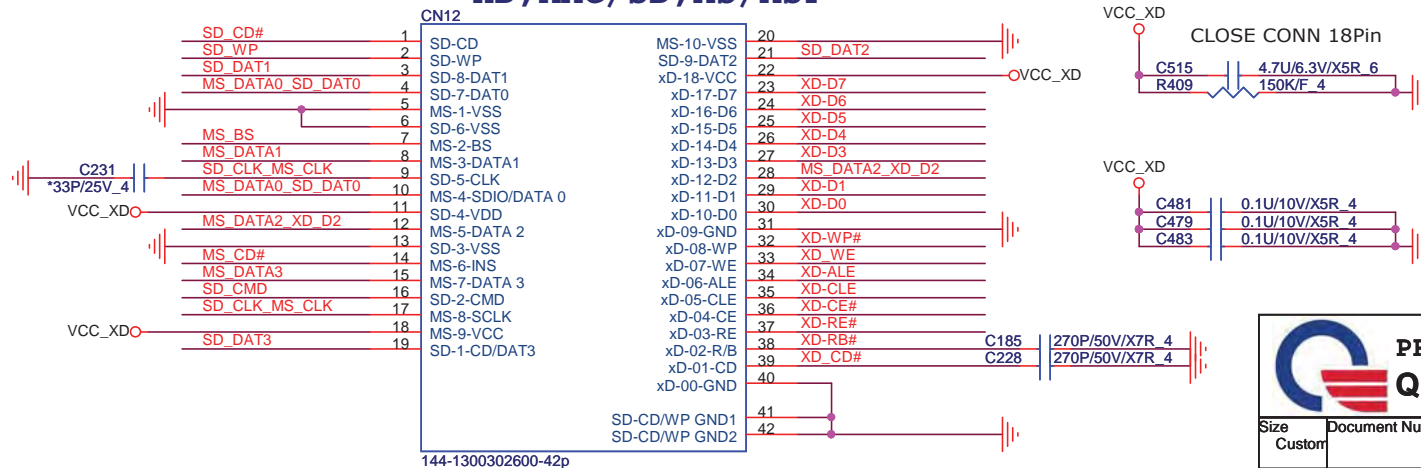


Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

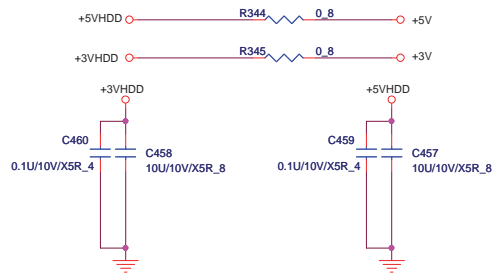
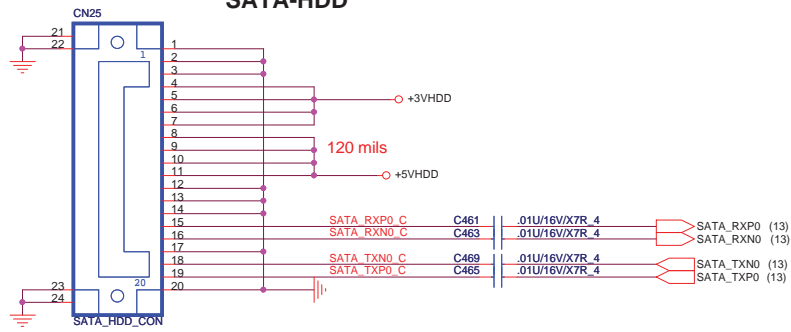


5 IN1 CARD READER XD, MMC/SD, MS/MSP

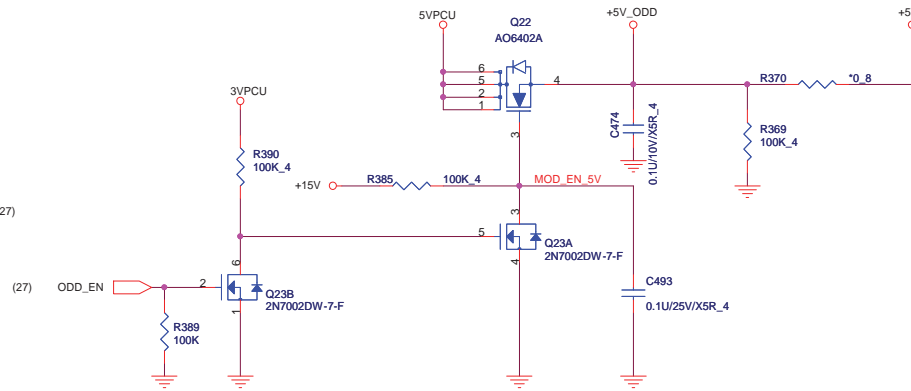
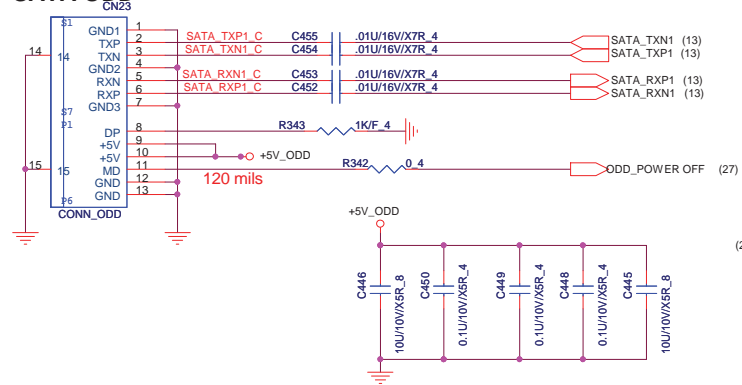



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		Quanta Computer Inc.	
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Custom			
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SATA-HDD

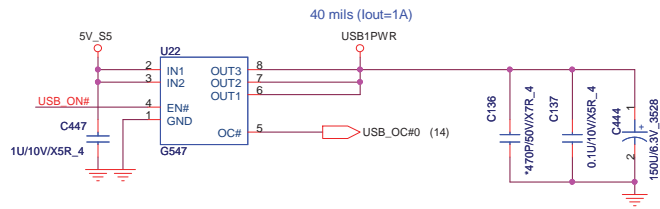


SATA ODD

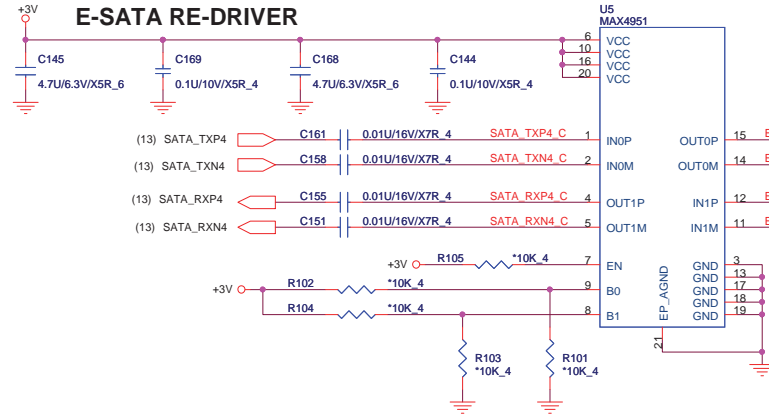


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	Quanta Computer Inc.	
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Custom	SATA HDD/ ODD/ eSATA/USB	1A
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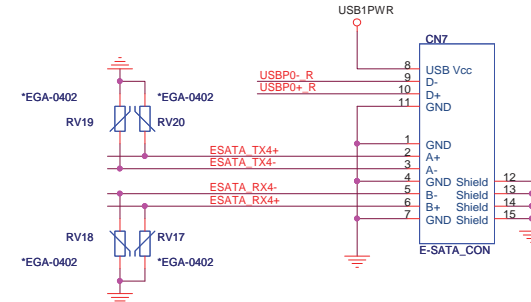
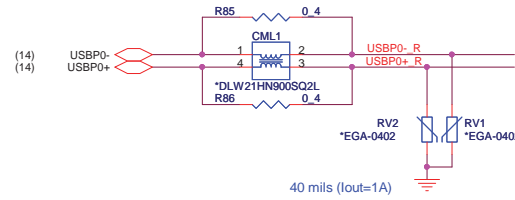
USB 1



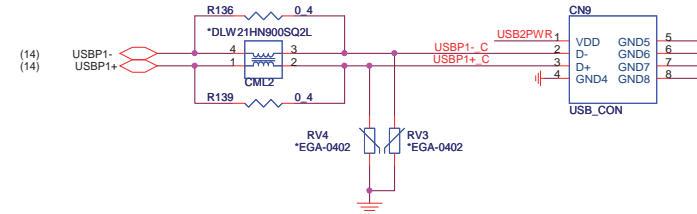
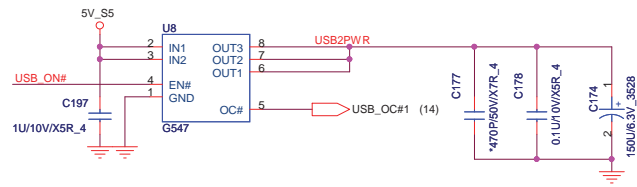
E-SATA RE-DRIVER



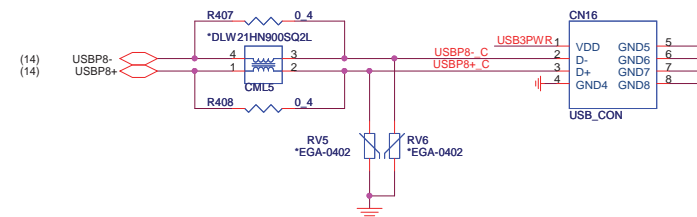
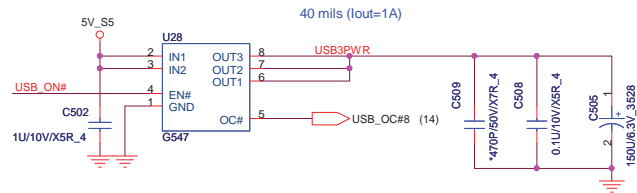
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



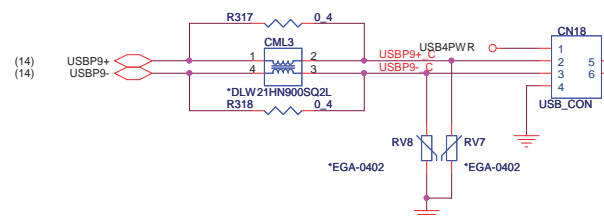
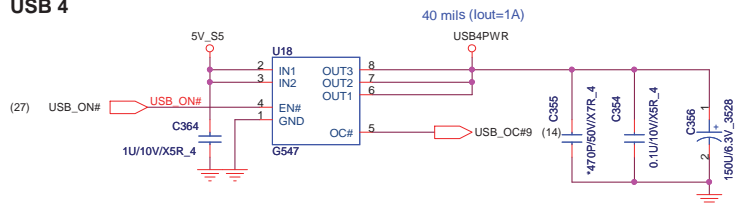
USB 2



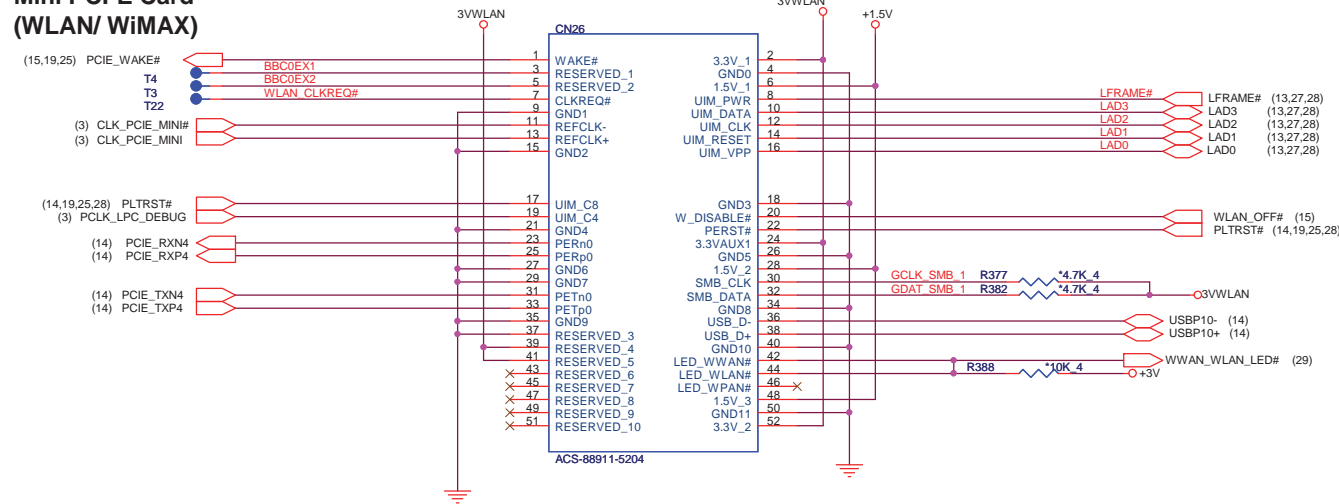
USB 3



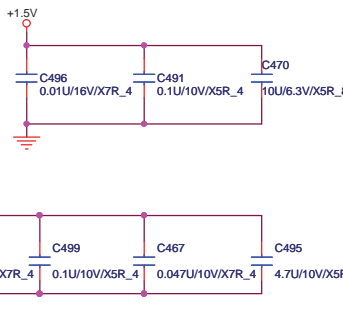
USB 4



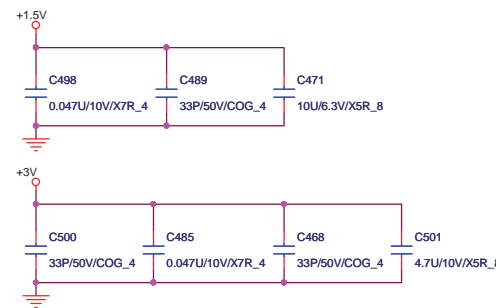
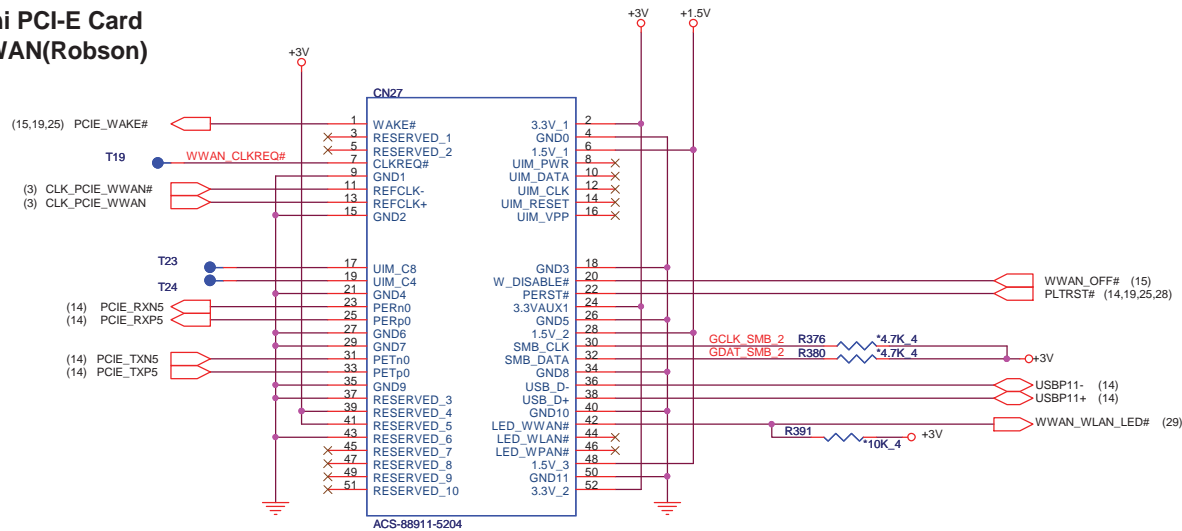
Mini PCI-E Card (WLAN/ WiMAX)



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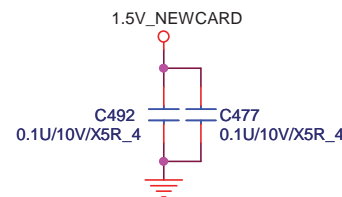
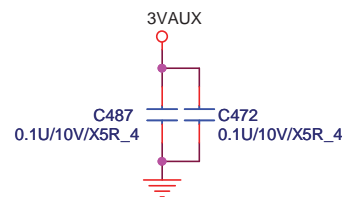
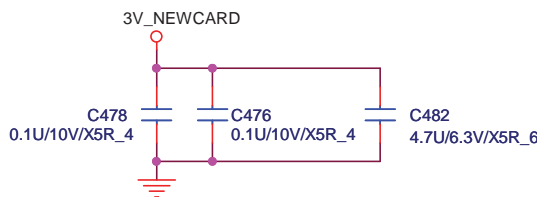
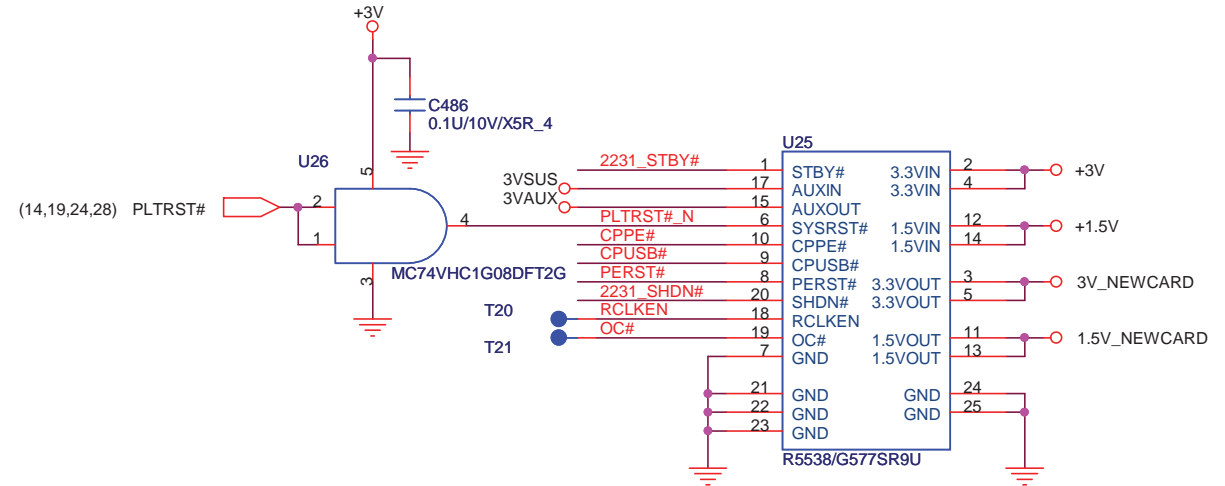
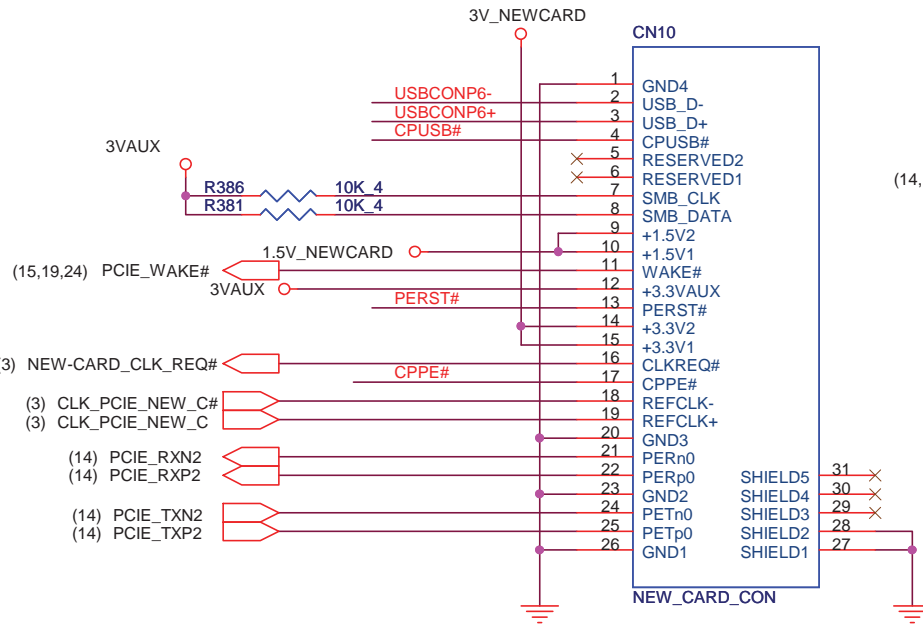
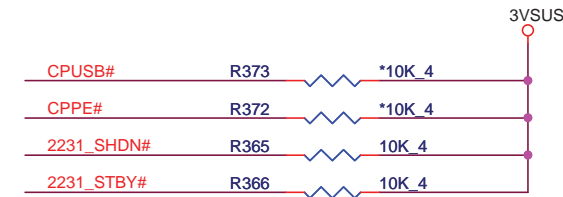
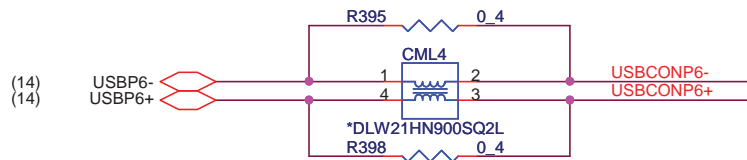



Mini PCI-E Card WWAN(Robson)



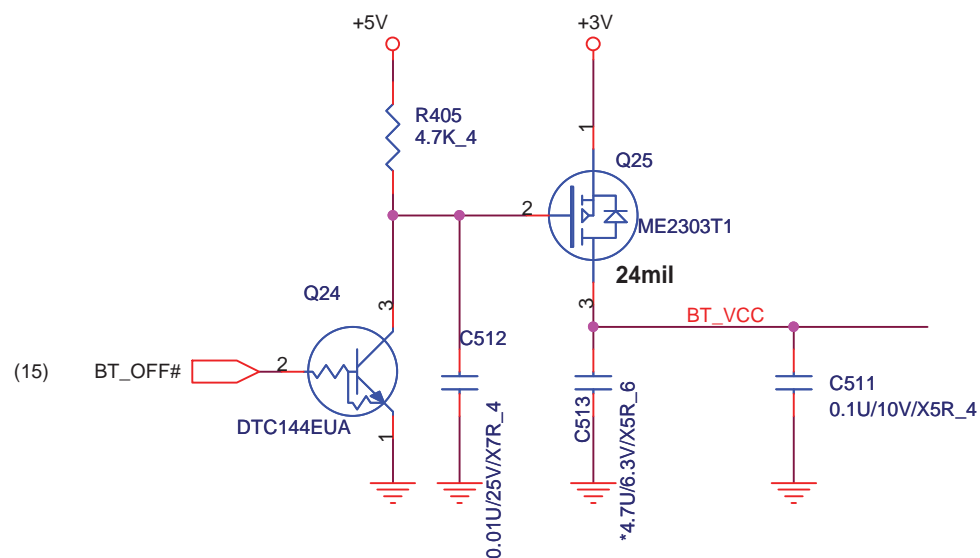
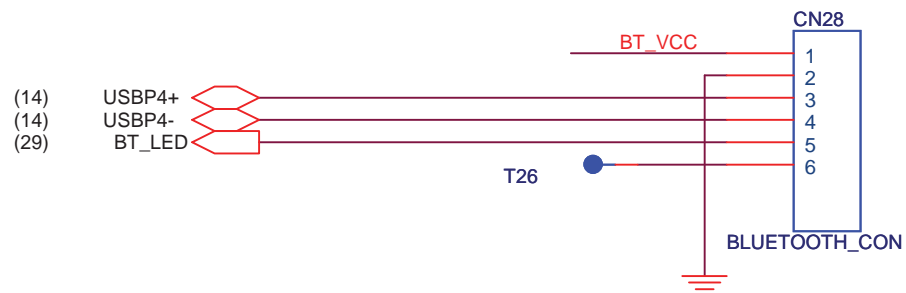
PCI Express Card

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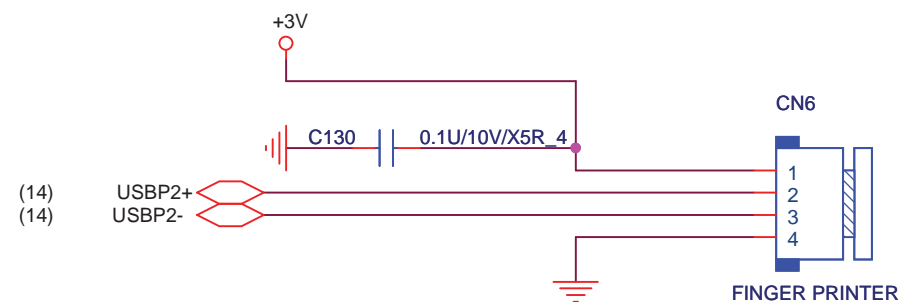



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BLUETOOTH

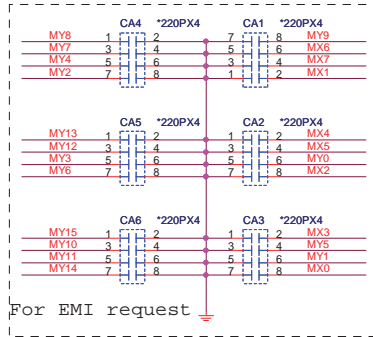
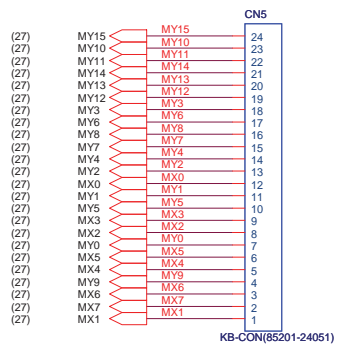


FINGER PRINTER

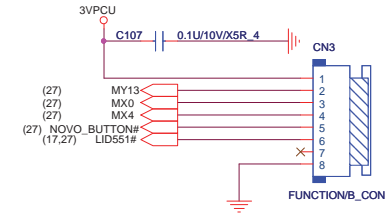


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		Quanta Computer Inc.	
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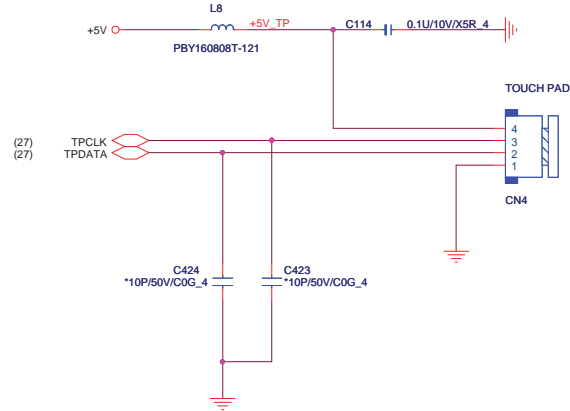
KEYBOARD



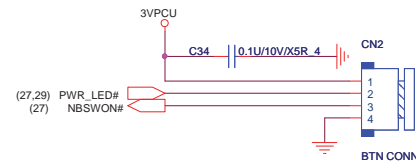
FUNCTION BUTTON BOARD



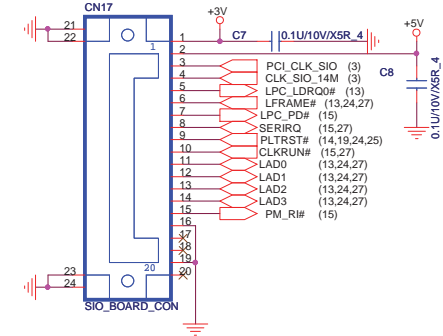
TOUCH PAD



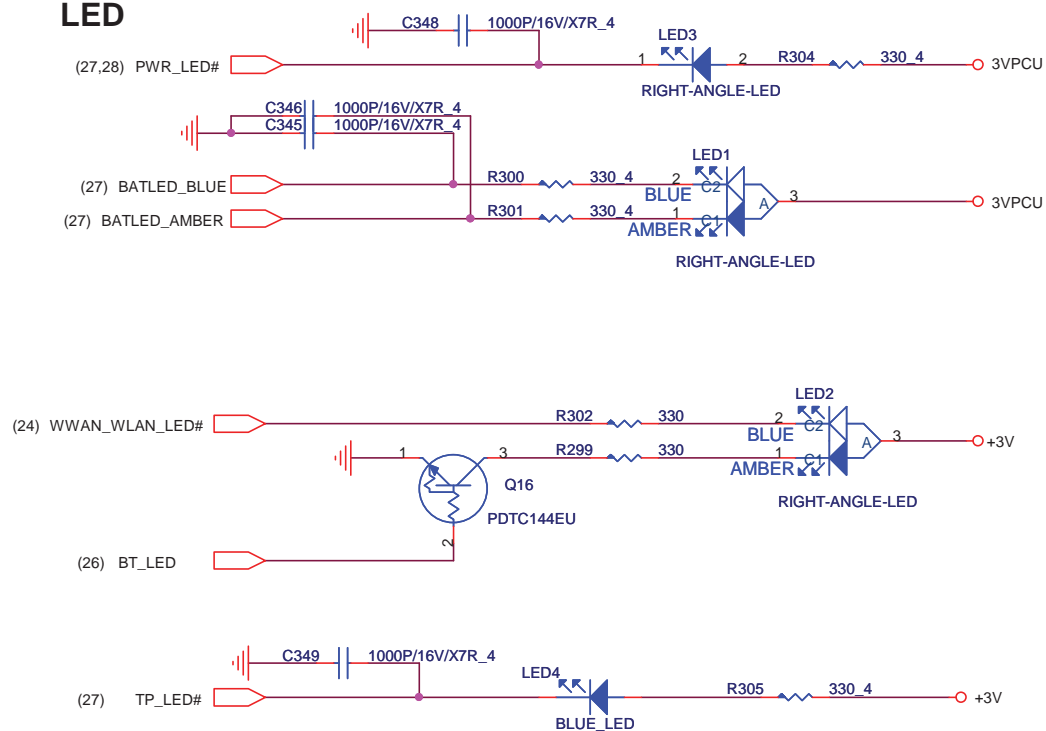
POWER BUTTON BOARD



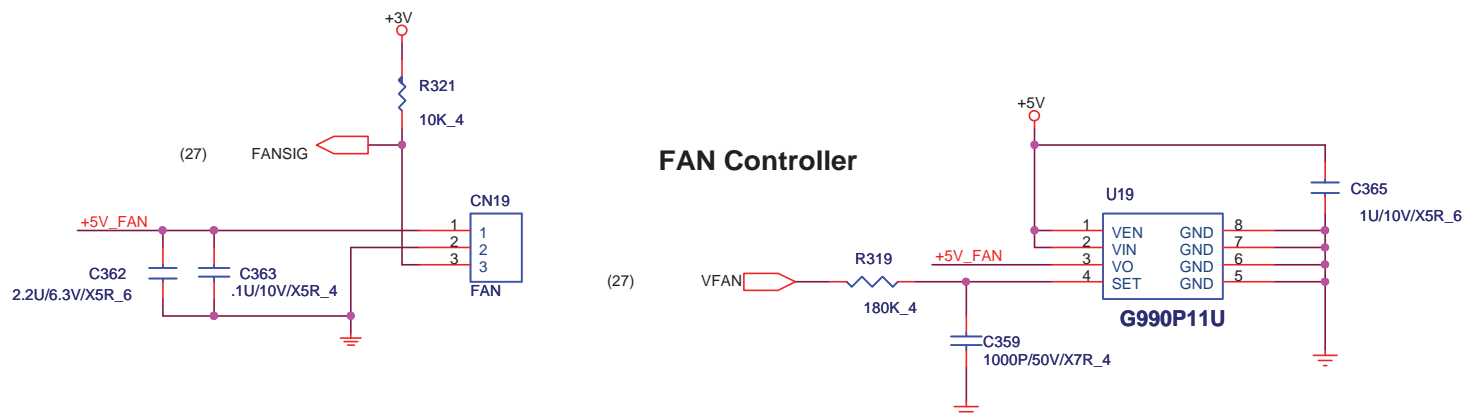
SIO BOARD



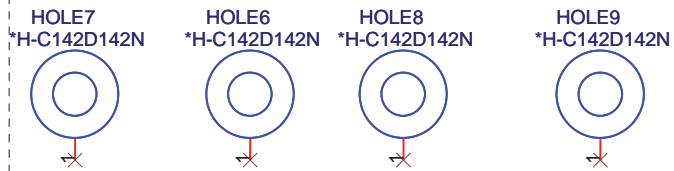
LED



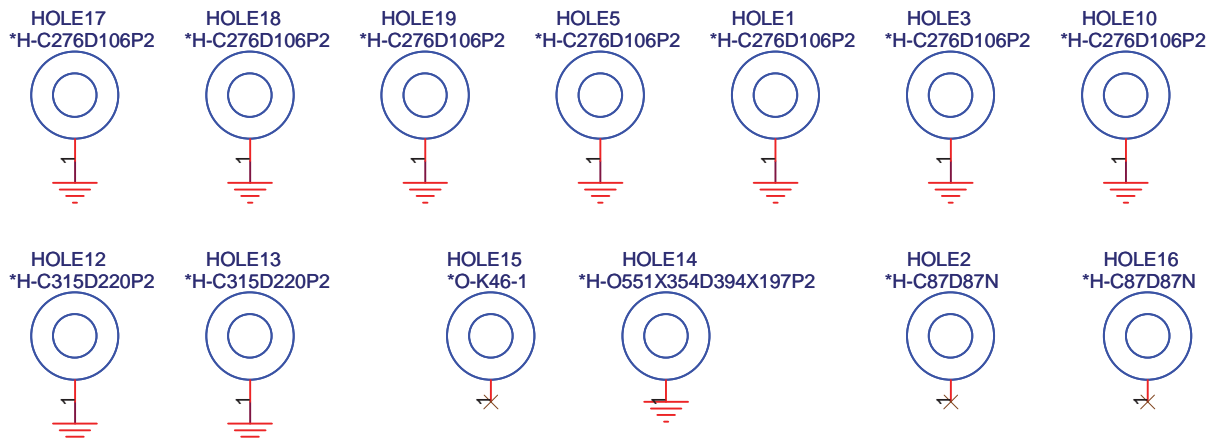
FAN Controller



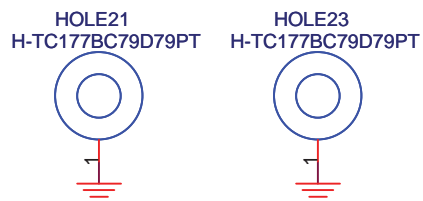
Hole for CPU support



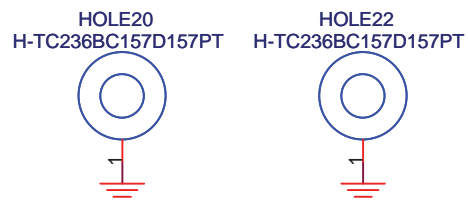
North Bridge nut



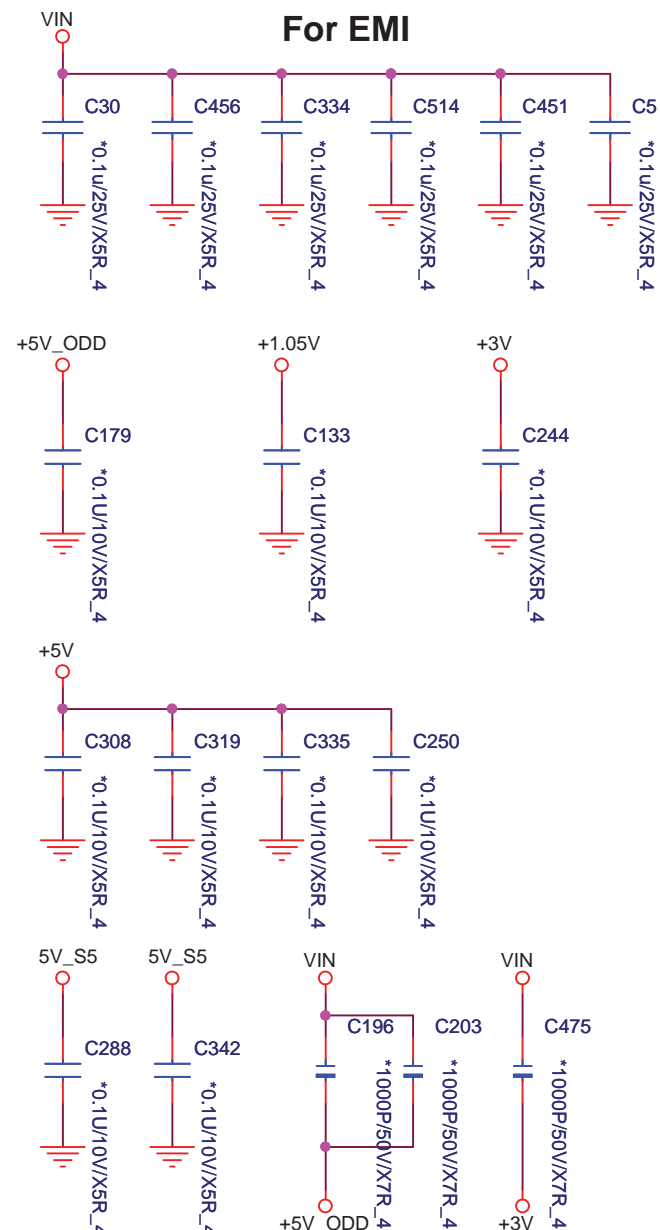
WWAN nut



WLAN nut



For EMI



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A

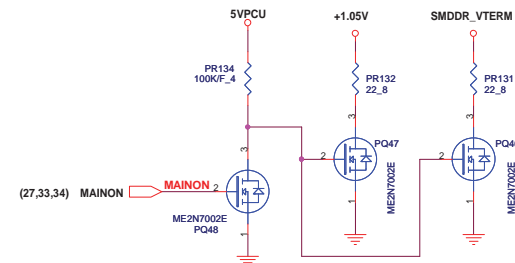
Document Number

KB/TP/FAN/SCREW HOLE

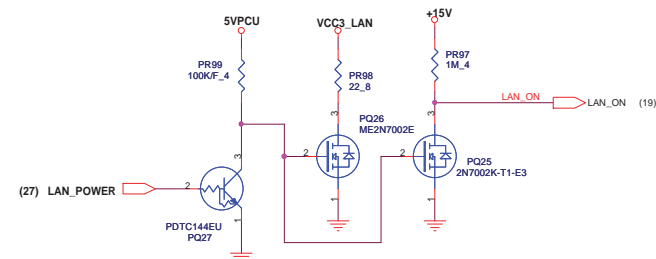
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LANVCC



VCC_CORE

